## Quantum Computer on a Chip

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## **Abstract**

Quantum computing is a new paradigm that exploits fundamental principles of quantum mechanics, such as superposition and entanglement, to tackle problems in mathematics, chemistry and material science that are well beyond the reach of supercomputers. Despite the intensive worldwide race to build a useful quantum computer, it is projected to take decades before reaching the state of useful quantum supremacy. The main challenge is that qubits operate at the atomic level, thus are extremely fragile, and difficult to control and read out. The current state-of-art implements a few dozen magnetic-spin based qubits in a highly specialized technology and cools them down to a few tens of millikelvin. The high cost of cryogenic cooling prevents its widespread use. A companion classical electronic controller, needed to control and read out the qubits, is mostly realized with room-temperature laboratory instrumentation. This makes it bulky and nearly impossible to scale up to the thousands or millions of qubits needed for practical quantum algorithms. We propose a new quantum computer paradigm that exploits the wonderful scaling achievements of mainstream integrated circuits (IC) technology which underpins personal computers and mobile phones. Just like with a small IC chip, where a single nanometer-sized CMOS transistor can be reliably replicated millions of times to build a digital processor, we propose a new structure of a qubit realized as a CMOS-compatible charge-based quantum dot that can be reliably replicated thousands of times to construct a quantum processor. Combined with an on-chip CMOS controller, it will realize a useful quantum computer which can operate at a much higher temperature of 4 kelvin.

## **Speaker**

R. Bogdan Staszewski received B.S. (summa cum laude), M.S. and PhD from University of Texas at Dallas, USA, in 1991, 1992 and 2002, respectively. From 1991 to 1995 he was with Alcatel in Richardson, Texas. He joined Texas Instruments in Dallas, Texas in 1995. In 1999 he co-started a Digital RF Processor (DRP) group in TI with a mission to invent new digitally intensive approaches to traditional RF functions. Dr. Staszewski served as a CTO of the DRP group between 2007 and 2009. In July 2009 he joined Delft University of Technology in the Netherlands where he is currently a part-time Full Professor. Since Sept. 2014 he is a Full Professor at University College Dublin (UCD) in Ireland. He has co-authored four books, seven book chapters, 260 journal and conference publications, and holds 180 issued US patents. His research interests include nanoscale CMOS architectures and circuits for frequency synthesizers, transmitters and receivers. He is an IEEE Fellow and a recipient of IEEE Circuits and Systems Industrial Pioneer Award (<a href="http://ieee-cas.org/about/awards/industrial-pioneer-award">http://ieee-cas.org/about/awards/industrial-pioneer-award</a>). He is a Technical Program Committee Chair of IEEE European Solid-State Circuits Conference (ESSCIRC) in 2019 in Krakow, Poland.